6 GND

5 I/O5



## Transil™ array for data line protection

#### **Features**

- High surge capability Transil array: I<sub>PP</sub> = 40 A (8/20 µs)
- Peak pulse power : 300 W (8/20 µs)
- Up to 6 bidirectional Transil functions
- Low clamping factor (V<sub>CL</sub> / V<sub>BR</sub>) at high current level
- Low leakage current
- ESD protection up to 15 kV

#### Complies with the following standards

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G- Method 3015-7: class 3B
  - 25 kV (human body model)

# Figure 1. Functional diagram I/O1 1 8 I/O6 I/O2 2 7 GND

**I/O4** 

## **Applications**

Data transmission lines protection, such as:

- Unipolar signal up to 5.5 V
- Bipolar signal in the ± 2.5 V range

### **Description**

Transil diode arrays provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages makes them particularly suited to protect voltage sensitive devices such as MOS technology and low voltage supplied IC's.

The ITA series allies high surge capability against energetic pulses with high voltage performance against ESD.

TM: Transil is a trademark of STMicroelectronics

Characteristics ITAxxU1

## 1 Characteristics

Table 1. Absolute ratings  $(T_{amb} = 25 \, ^{\circ}C)$ 

Symbol	Parameter	Value	Unit	
P <sub>PP</sub>	Peak pulse power (8/20 μs) <sup>(1)</sup>	300	W	
I <sub>PP</sub>	Peak pulse current (8/20 μs) <sup>(1)</sup>	$T_j$ initial = $T_{amb}$	40	Α
I <sup>2</sup> t	Wire I <sup>2</sup> t value <sup>(1)</sup>	0.6	A <sup>2</sup> s	
T <sub>j</sub>	Maximum operating junction temperature	125	°C	
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C	
TL	Maximum lead temperature for soldering during 10 s	260	°C	

<sup>1.</sup> For surges greater than the specified maximum value, the I/O will first present a short-circuit and after an open circuit caused by the wire melting.

Table 2. Electrical characteristics ( $T_{amb} = 25 \,^{\circ}C$ )

Table 2.	Liectrical characteristics (1 <sub>amb</sub> = 25 °C)											
Symbol	Parameter							1+				
$V_{RM}$	Stand-off voltage								IF			
$V_{BR}$	Breakdown voltage											
V <sub>CL</sub>	Clamping voltage				V <sub>BR</sub> V <sub>F</sub>							
I <sub>RM</sub>	Leakage current					VcL↓	V <sub>RM</sub>	I <sub>RM</sub>		→V		
I <sub>PP</sub>	Peak pulse current											
αТ	Voltage	tempera	ture coe	fficient								
V <sub>F</sub>	Forward voltage drop					Ipp						
С	Capacita	ance					•		I			
	V <sub>BR</sub>	@ I <sub>R</sub>	I <sub>RM</sub> @	V <sub>RM</sub>	V <sub>CL</sub>	@ I <sub>PP</sub>	V <sub>CL</sub>	@ I <sub>PP</sub>	α <b>T</b>	С	V <sub>F</sub>	@ I <sub>F</sub>
Order code	min.				max.	8/20 µs	max.	8/20 μs	max.	max.	max.	
Gluer coue	(1)		max.		(1)		(1)			(2)		
	V	mA	μΑ	V	V	Α	V	Α	10 <sup>-4</sup> / °C	pF	V	Α
ITA6V1U1	6.51	1	10	5	10	10	12	25	4	1500	1.3	1

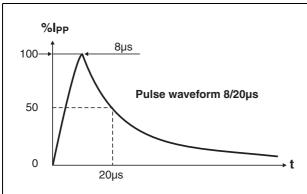
<sup>1.</sup> Between I/O pin and ground.

<sup>2.</sup> Between two input pins at 0 V Bias, F = 1 MHz.

ITAxxU1 Characteristics

Figure 2. Pulse waveform

Figure 3. Typical peak pulse power versus exponential pulse duration



Ppp(W)

1000

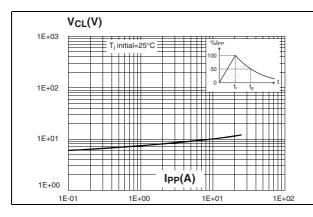
tp(ms) expo

10

1E-3 1E-2 1E-1 1E+0 1E+1

Figure 4. Clamping voltage versus peak pulse current (exponential waveform 8/20 µs)

Figure 5. Peak current I<sub>DC</sub> inducing open circuit of the wire for one input/output versus pulse duration (typical values)



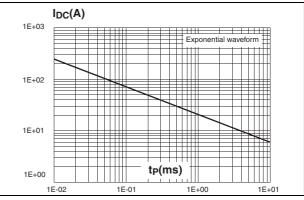
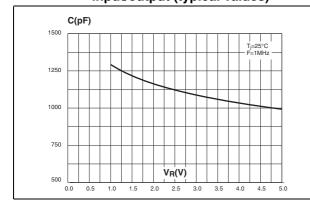
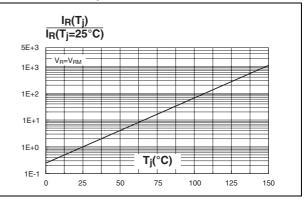


Figure 6. Junction capacitance versus reverse applied voltage for one input/output (typical values)

Figure 7. Relative variation of leakage current versus junction temperature





# 2 Application information

Figure 8. µP I/O lines

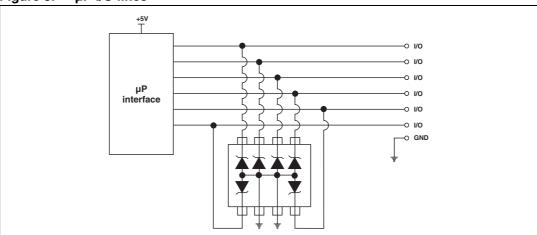
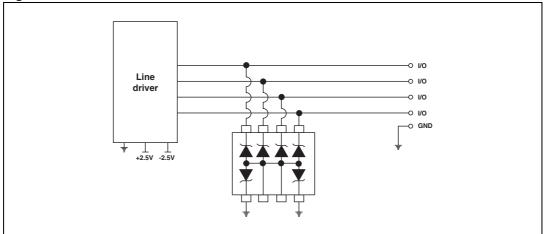
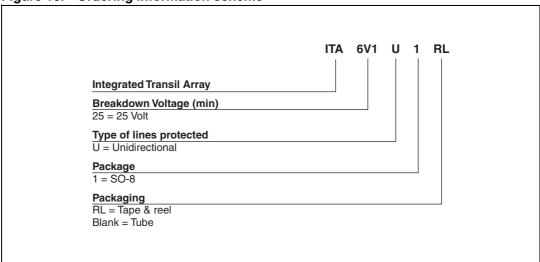


Figure 9. ± 2.5 V datalines



## 3 Ordering information scheme

Figure 10. Ordering information scheme



Package information ITAxxU1

## 4 Package information

#### Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 3. SO-8 dimensions

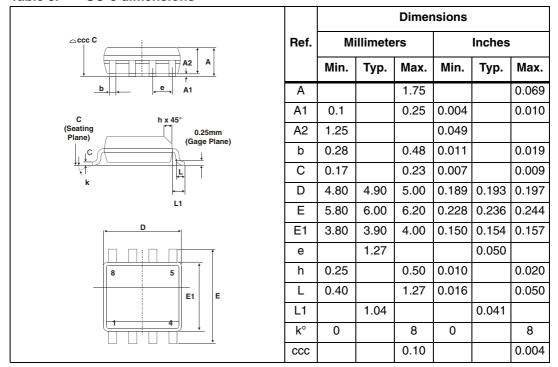
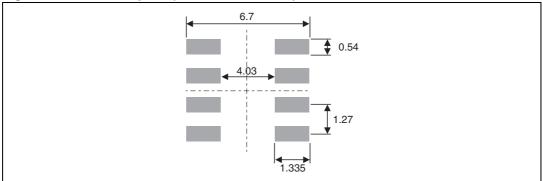


Figure 11. SO-8 footprint (dimensions in mm)



# 5 Ordering Information

Table 4. ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ITA6V1U1	6V1U1	SO-8	0.08 g	2000	Tube
ITA6V1U1RL	6V1U1	30-0	0.06 g	2500	Tape and reel

# 6 Revision history

Table 5. Document revision history

Date	Revision	Changes
13-Dec-2004	1	Initial release.
07-Nov-2007	2	Reformatted to current standards. SO-8 package dimensions update.

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